

DENSITY OF INTERFACE STATES AT THE SILICON-SILICON DIOXIDE INTERFACE OF TEXTURED SILICON WITH RANDOM PYRAMIDS

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ABSTRACT

The aim of this work was to measure the density of states (D_{it}) at the interface between SiO_2 and silicon textured with random pyramids. Previous research has measured the surface recombination velocity at the Si- SiO_2 interface of textured samples using photoconductance, but in this work the recombination is examined in more detail by measuring the defect density as a function of energy using capacitance-voltage (C-V) measurement. Initially the C-V measurements on textured samples were unsuccessful due to prohibitive leakage through the oxide. The leakage was reduced by a rounding etch on the textured silicon to enable a measurement of D_{it} . The D_{it} values for these near-textured surfaces were approximately 8-10 times greater than their equivalent planar surfaces. Photoconductance, reflectance and scanning electron microscope (SEM) images were also used to evaluate the samples.

1. INTRODUCTION

Glunz *et al.* [1] and King *et al.* [2] have determined the surface recombination velocity at the Si- SiO_2 interface and the emitter saturation current density (J_{0e}) of textured samples. King *et al.* found that for an emitter thickness of 1 μm and a surface concentration of $1 \times 10^{19} \text{ cm}^{-3}$ the J_{0e} changed from 35 $\text{fA/cm}^2/\text{side}$ for planar up to 80 $\text{fA/cm}^2/\text{side}$ for textured surfaces. This equates to an increase of 2-3 times for textured over planar surfaces. Kerr *et al.* also quotes textured surfaces having ~ 3 times greater J_{0e} for a similar oxide and sheet resistance range [4].

To our knowledge, the D_{it} at the Si- SiO_2 interface of textured silicon has not previously been measured. A knowledge of D_{it} and how it depends on processing may help improve the understanding of surface recombination for high-efficiency solar cells. The aim of this work was to develop a method for measuring D_{it} values on textured silicon surfaces using capacitance-voltage (C-V) measurements. Photoconductance, reflectance, and SEM images were also used to evaluate the samples.

2. EXPERIMENTAL

The procedure is illustrated in Figure 1. There were three sets of samples prepared. Set A for C-V, set B for photoconductance and set C for SEM and reflectance measurements.

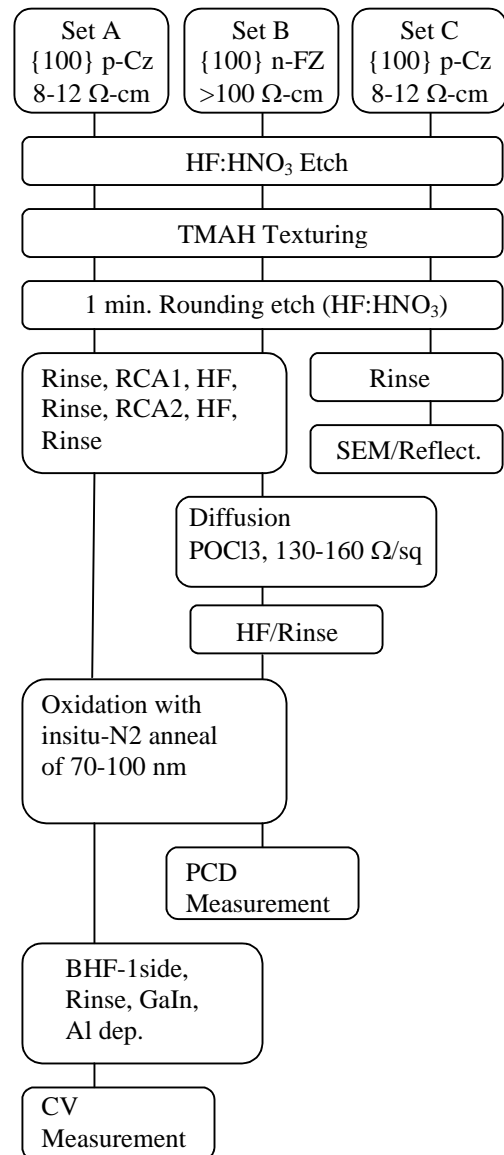


Figure 1: Experimental procedure.

After texturing, the samples received a rounding etch to varying degrees. This provided a range of texturing, from perfectly formed pyramids to almost completely planar samples.

Following the texturing, Set A were cleaned, oxidised, and fabricated into MOS capacitors by removing the rear oxide, evaporating a 0.0775 cm diameter aluminum contact of 7-8 nm thickness onto the front oxide, and depositing a gallium indium eutectic paste to the rear. For the measurement, a HP4284A High Frequency (HF) meter connected to a HP4140B Quasi-Static (QS) was used. Both were in one unit developed by the Materials Development Corporation (USA). The method used to extract the D_{it} was the Castagne method [3] and the gate voltage sweep rate used was 0.1 V/s. Set B were lightly diffused with $POCl_3$ prior to the oxidation to enable the measurement of a J_{0E} value with photoconductance decay. Set C were used for reflectance and SEM imaging.

3. RESULTS & DISCUSSION

C-V measurements on samples with no rounding etch could not be attained due to leakage through the oxide insulator. It was, however, possible to attain data on samples that had a very light rounding etch (1:60 HF:HNO₃) and all samples with higher etch concentrations. The resultant D_{it} values, plotted in Fig. 2, increase with decreasing surface rounding. The near-textured surface had a D_{it} of 8-10 times their planar counterparts.

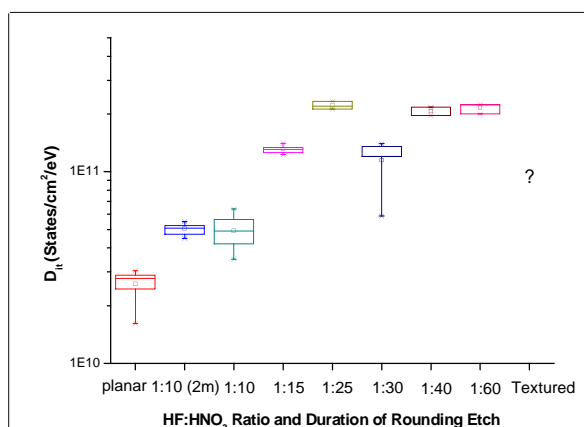


Figure 2: D_{it} (states/cm²/eV) at midgap for the same surfaces. Textured samples without a rounding etch could not be measured. Statistical box plots are used.

The J_{0E} values from the photoconductance measurements ranged from 20 fA/cm²/side for planar surfaces through to 106 fA/cm²/side for textured surfaces. This 5 times increase in J_{0E} is greater than that found by with King *et al.* [2].

The SEM images showed evidence of rounding peaks and troughs at low etch concentrations, and practically planar surfaces at high concentrations. Figure 3 provides example images.

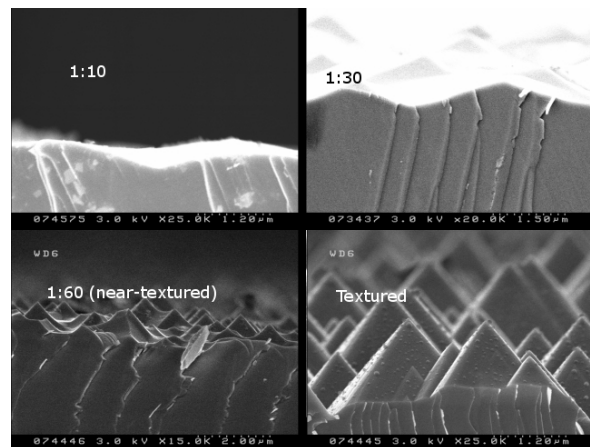


Figure 3: SEM images of 1:10, 1:30, 1:60 HF:HNO₃ etched (near-textured) and Textured Surfaces.

4. CONCLUSIONS

This work was able to determine that adverse leakage currents prevent textured surfaces being measured with C-V. Near-textured surfaces were measured, however, and found to have a D_{it} of 8-10 times greater than their planar counterparts. Photoconductance, reflectance and SEM images were also used to evaluate the samples. The J_{0E} of textured samples were ~5 times higher than their planar counterparts.

5. ACKNOWLEDGEMENTS

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