SURFACE PASSIVATION ATTAINED BY SILICON DIOXIDE GROWN AT LOW TEMPERATURE IN NITRIC ACID

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ABSTRACT: This work investigates silicon dioxide (SiO_2) layers grown at low temperature in concentrated nitric acid (HNO_3) solutions. This procedure has the potential to be significantly less expensive than the thermal oxides used in high-efficient solar cells and test structures, but it must also provide good surface passivation. The SiO_2 layers are formed by two methods. The first method involves growing a thin (5 nm) SiO_2 layer by a two-step nitric acid oxidation process developed by Imai *et al.* for thin film transistors. The second being a direct current anodization (DCA) process using a 5 wt% HNO_3 solution, which results in an SiO_2 thickness of 40 nm. Prior to an anneal, both oxidation processes do not passivate the silicon surface, however after an 1100 °C N_2 anneal for 30 mins, SRV of 107 cm/s and 70 cm/s can be achieved respectively. The SRV can be further decreased to 40 cm/s after a 30 min forming gas anneal (FGA) at 400 °C. However, the DCA oxides only require a 900 °C N_2 anneal for 30 mins to achieve an SRV of 80 cm/s. Thus, while both processes provide high quality SiO_2 after a high temperature anneal, the DCA process shows more potential due to the ability to grow thicker SiO_2 layers with more control, which passivate at lower annealing temperatures.
Keywords: SiO_2, Passivation, Surface Recombination Velocity

1 INTRODUCTION

The passivation attained by a thermal silicon dioxide (SiO_2) layer on silicon (Si) is well known to lead to a low surface recombination velocity (SRV). An SRV of ~30 cm/s has been attained after a post oxidation anneal in argon and forming-gas [1], however as such high temperatures and long oxidation times are required, the process to achieve low SRV is expensive relative to the cost of modern solar cell processing. Therefore new and inexpensive methods to grow high-quality SiO_2 are desired. One method to grow inexpensive SiO_2 has been recently developed by Imai et al. [2]. They first immerse silicon into a 40 wt% nitric acid (HNO_3) solution at ~110 °C for 10 mins, which forms ~ 1 nm thick SiO_2 layer. The sample is then immersed in 68 wt% HNO_3 solution at ~ 120 °C for 2–4 hours, which further increases the SiO_2 thickness to 3–7 nm. Another method to grow thicker (40 nm) SiO_2 layers is by a direct current anodization (DCA) process, where a positve bias is applied to a silicon wafer in a very low concentrated HNO_3 solution at room temperature.

This paper characterises the SiO_2 grown by both chemical oxidation methods after 1) no anneal, 2) a nitrogen (N_2) anneal and 3) a N_2 anneal followed by a forming gas anneal (FGA). Photoconductance measurements are conducted to determine the SRV of the samples, and capacitance-voltage (C-V) measurements are conducted to assess the density of interface states and charge density.

2 SAMPLE FABRICATION

The two-step nitric oxidation was evaluated on 200 µm thick, 100 mm diameter, single crystalline, (100) oriented, FZ 1 Ωcm n-type silicon wafers, while the DCA oxidation was evaluated on 700 µm thick 5 Ωcm n-type silicon wafers. Prior to the oxidations, all wafers received an HF:HNO_3 etch for three minutes to remove saw damage from the surfaces and cleaned by the conventional RCA procedure [3].

The two-step nitric acid SiO_2 layers were grown by immersing the samples in a 40 wt% HNO_3 solution at 108 °C for 10 mins followed by a 3 hour immersion in 68 wt% HNO_3 solution at 121 °C, resulting in an oxide thickness of ~ 5 nm. The DCA formed SiO_2 layers were grown by applying a positive 25 volt bias across two silicon wafers immersed in a 5 wt% HNO_3 solution, where the wafer held at the higher potential formed a 40 nm SiO_2 layer. Some wafers were subsequently annealed in a tube furnace at 400 °C, 700°C, 800 °C, 900 °C and 1100 °C in N_2 for 30 mins with and without a subsequent FGA at 400 °C for 30 mins.

3 RESULTS

3.1 Photoconductance Measurements

The SRV was determined from photoconductance measurements using a generalised analysis [4]. Two light sources were employed: a Quantum Q-flash X2 lamp used in the WCT-100 instrument [5], and an LED array of wavelength, 870 nm. The LED array had several advantages over the Q-flash: it operated at one wavelength, simplifying the analysis, the pulse shape was controlled to permit rapid averaging, and a self-consistent technique could be applied to calibrate the light intensity [6], [7]. It could not, however, attain as high an illumination intensity as the Q-flash. The photogeneration rate from the flash source was corrected to agree with that of the more accurately calibrated LED source.

The SRV plotted in Fig. 1 were calculated from the effective lifetime accounting for the non-uniform carrier concentration in the wafer and assuming an infinite bulk lifetime. The SRV is therefore an upper limit to its actual value, but would overestimate SRV by no more than 18% if the bulk lifetime were 2 ms (a more realistic lifetime of FZ silicon). The figure indicates that at $\Delta n = 10^{15}$ cm^{-3}, an SRV of less than 42 cm/s was achieved after annealing at 1100 ºC in N_2 followed by a 400 ºC FGA. This compares to an SRV of ~30 cm/s at the same injection level for a thermal oxide grown at 1050 ºC with a post-oxidation anneal in argon for 1 hour followed by a 450 ºC FGA [1]. Unfortunately the improvement in surface passivation achieved by the FGA is temporary, presumably due to the instability of

the Si–H bond [8], resulting in an increase in the lowest SRV from 42 cm/s to 82 cm/s at $\Delta n = 10^{15}$ cm^{-3} 1 month after the anneal.

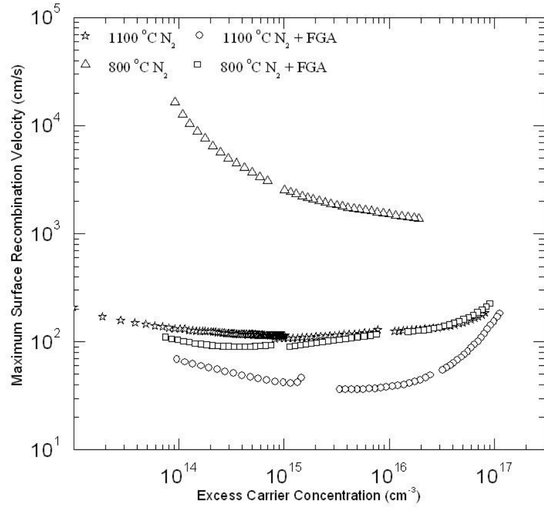

Fig. 1. The maximum SRV directly after the annealing process. For clarity, the figure plots every fifth data point. The wafer substrates were FZ, (100), 1 Ωcm, n-type with a thickness of 200 μm

3.2 C-V Measurements For The Two-Step Nitirc Acid SiO_2 Layers

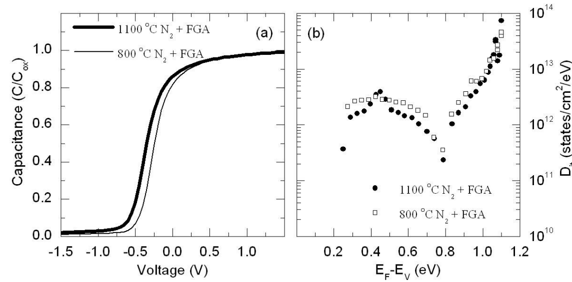

Fig. 2. (a) C-V curves after annealing at 800 ºC and 1100 ºC in N_2 followed by a 400 ºC FG anneal, and (b) the corresponding density of interfacial defects as determined by a Terman analysis.

C-V curves were recorded at 1 MHz using a 4284A Precision LCR meter. The measurements were hampered by significant leakage through the thin oxide, limiting the D_{it} analysis to only those samples that had an anneal in N_2 and a subsequent FGA, indicating that the leakage is dependent on the passivation of interface states, in agreement with the results of Kobayashi *et al* [9] and Imai *et al* [2]. The C-V curves presented in Fig. 2(a) are those of the samples annealed at 800 °C and 1100 °C in N_2 followed by a 400 °C FGA. They show two interesting effects: the first is a voltage translation, which relates to a difference in oxide charge density Q_{ox}; and the second is their similar shape, which indicates a similar density of interface states D_{it}.

Oxide fixed charge is located near the Si/SiO_2 interface and can be either positive or negative, however for thermal oxides, positive charge is the more common [10]. If the charge in our samples were located at the interface itself, the shift in flat-band voltage equates to Q_{ox} of the 1100 °C sample being 7×10^{11} $cm^{-2} \pm 30\%$ more positive than Q_{ox} of the 800 °C sample.

While there is a clear difference in Q_{ox} between the C-V curves, their shape is very similar, implying their D_{it} is also similar. Fig. 2(b) plots D_{it} as a function of energy above the valence band as calculated by Terman's analysis [11], indicating that the 1100 °C sample has only slightly fewer interface states than the 800 °C sample.

We conclude from the C-V measurements that the lower SRV attained at higher temperatures relates mostly to more positive fixed charge rather than a lower D_{it}.

3.3 Surface Passivation vs Immersion Time In The 68 wt % HNO_3 Solution

In previous work on thin SiO_2 layers grown in nitric acid, the growth rate depended linearly on immersion time in the 68 wt% HNO_3 solution [12]. Here, we investigate how SRV depends on immersion time. Fig. 3 plots the results for both n- and p-type silicon of low and high resistivity after an 1100 °C N_2 anneal. It shows that SRV decreases rapidly for short immersion times and saturates after 3–4 hours.

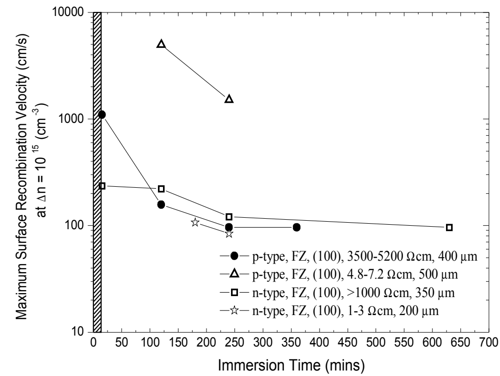

Fig. 3. SRV as a function of immersion time, where the shaded area corresponds to the time spent in the 40 wt% nitric acid solution. The unshaded area corresponds to the immersion time in the 68 wt% nitric acid solution after being immersed in the 40 wt% solution. All samples received an 1100 ºC N_2 anneal for 30 minutes but not an FGA

The figure also shows that SRV depends on substrate doping, most likely due to the positive Q_{ox} at the interface as now explained. On low resistivity p-type silicon, the positive charge attracts minority carriers (electrons) and repels the majority carriers (holes), increasing the recombination rate and therefore the SRV, due to insufficient inversion at the interface [10]. On high-resistivity (near intrinsic) p-type silicon, the positive charge is sufficient to cause substantial inversion, and the samples behave similarly to those of high-resistivity n-type; i.e., the dopant concentration in these samples is too low to affect the measurements. On low-resistivity n-type, the positive charge repels minority carriers (which were already low to begin with), making the recombination rate still lower. This dependence of SRV on substrate doping would be exacerbated by the asymmetric capture cross sections frequently observed at SiO_2–Si interfaces, whereby the electrons are more readily captured than holes [13].

3.4 Two-Step vs One-Step Nitric Acid Oxidation of Silicon

Thermally grown SiO_2 layers have been shown to improve surface passivation with oxide thickness [14].

Here we investigate how surface passivation varies under different oxidation conditions and hence, different oxide thicknesses. The two-step oxidation process is as described above, with an oxide thickness of ~ 5 nm, whereas the one-step method involves immersing the substrate in a 68 wt% HNO_3 solution at 30 °C for 15 mins. The SiO_2 layer was assumed not to be any thicker than 1.5 nm, and has been shown not to increase with further immersion [9].

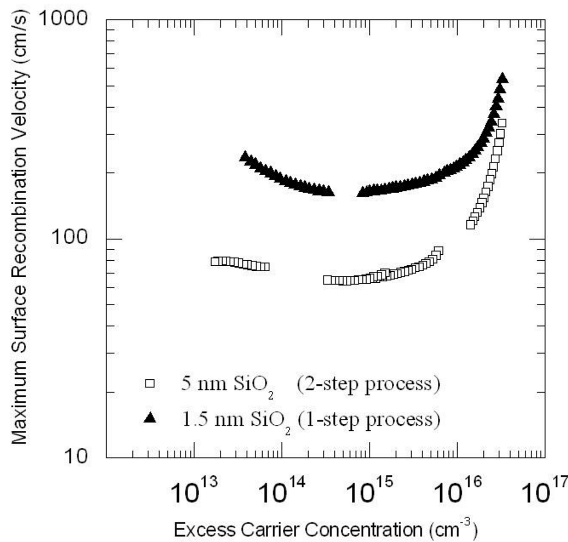

Fig. 4. The maximum SRV of the two different oxidation processes after an 1100 °C N_2 anneal for 30 minutes. For clarity, the figure plots every fifth data point. The wafer substrates were FZ, (100), 5 Ωcm, n-type with a thickness of 700 μm

As seen in Fig. 4, after an 1100 °C N_2 anneal for 30 minutes, the SRV of the 5 nm SiO_2 layer is half that of the 1.5 nm oxide. This most likely relates to a higher positive fixed charge in the 5 nm oxide rather than a reduction in the D_{it} as investigated by Grant *et al* [15]. However due to the ultra-thin (1.5 nm) SiO_2 layer formed during the one-step oxidation process, reliable C-V measurements could not be obtained due to high leakage currents through the oxide, and therefore the exact reason for the variation in the surface passivation is not known.

3.5 DCA of Silicon

DCA of silicon is a process that involves applying a voltage across two electrodes that are immersed in an electrolytic solution, where one electrode is usually made of metal (mainly platinum) and the other, a silicon substrate to be oxidized [2]. In our investigation of electrochemically formed SiO_2 layers, no metal is required. Thick (40 nm) SiO_2 layers can be formed by applying a positive voltage across two silicon wafers immersed in a 5 wt% HNO_3 solution at room temperature, where the substrate held at the higher potential grows the SiO_2 layer. The fact that the SiO_2 layer grows on the substrate held at the higher potential suggests that the oxidizing species are anions.

Here we investigate the passivation of the 40 nm thick electrochemically formed SiO_2 layers after various high temperature anneals, as no passivation is obtained directly after the oxidation.

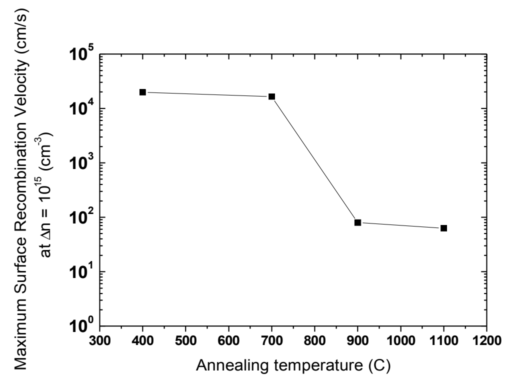

Fig. 5. The maximum SRV of a 40 nm DCA SiO_2 layer after a 30 min N_2 anneal at various temperatures.

Fig. 5 shows that a significant reduction in the SRV can be obtained by a 30 min N_2 anneal at 900 °C, indicating that bewteen 700 °C and 900 °C a significant change at the interface occurs. However as with the two-step nitric acid oxides, an 1100 °C N_2 anneal provides the best surface passivation, most likely casued by a large positive charge at the interface as observed in the nitric acid oxides [15].

3.6 SRV of DCA SiO_2 Layers After A 30 Minute FGA

Unlike the two-step nitric acid oxides, the SRV of the DC anodized samples is significantly reduced after a 30 min FGA at 400 °C. The reduction in SRV is thought to be due to a reduction in interfacial defects by hydrogen rather than an increase in positive charge at the interface. This assumption is supported by the fact that a 400 °C N_2 anneal did not provide any surface passivation.

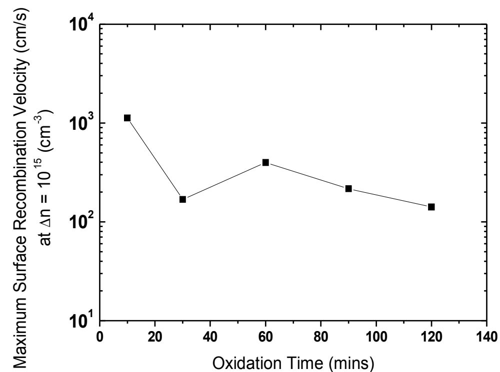

Fig. 6. The maximum SRV after a 30 min FGA as a function of DCA oxidation time.

Fig. 6 illustrates that as oxidation time is increased, and hence as oxide thickness increases, the SRV begins to saturate at an average value of 200 cm/s.

4 CONCLUSION

This paper presented a study into the SRV attained by nitric-acid oxides. Without an anneal, Imai *et al.*'s two-step nitric oxide offered poor passivation, but after a high-temperature anneal in N_2 and an FGA, an SRV of 42 cm/s (at $\Delta n = 10^{15}$ cm^{-3}) was attained, similar to that of a thermal oxide. C-V and photoconductance measurements suggest the oxides contain a high positive

fixed charge—particularly after an 1100 ºC N_2 anneal—which aids the passivation of n-type and intrinsic silicon but harms the passivation of low-resistivity p-type silicon. It was also shown that the SRV saturates after 3–4 hrs of immersion in the 68 wt% nitric acid solution and that the benefit of the FGA is mitigated over time. It was also demonstrated that while the one-step oxidation process is quick, its SRV is double that of the two-step oxidation process after a high temperature N_2 anneal.

Investigation of electrochemically formed SiO_2 layers by DCA has shown that oxide thicknesses of 40 nm can be formed, and that the SRV can be significantly reduced after a 30 min 900 ºC N_2 anneal. It was also discovered that unlike the nitric acid oxides, the SRV of the electrochemical SiO_2 layers is significantly reduced after a 30 min FGA at 400 ºC.

Therefore, while both oxidation processes provide good surface passivation after a high temperature anneal, the DCA process has more potential due to the ability to grow thicker SiO_2 layers at room temperature with more control, which passivate at lower annealing temperatures.

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