Passivation of a (100) Silicon Surface by Silicon Dioxide Grown in Nitric Acid

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Abstract—**This letter investigates silicon dioxide layers grown at low temperature in concentrated nitric acid using a two-step process developed by Imai *et al.* for thin-film transistors. With photoconductance measurements, we find that, prior to an anneal, nitric acid oxidation does not passivate the silicon surface, but, after a 30-min nitrogen anneal at 1100 °C, a surface recombination velocity (SRV) of 107 cm/s (at $\Delta n = 10^{15}$ cm^{-3}) is attained on 1-$\Omega \cdot$ cm n-type silicon. The SRV is further decreased to 42 cm/s after a 30-min forming gas anneal (FGA) at 400 °C, which is equivalent to a thermal oxide under similar annealing conditions, although it is not stable and returns to its pre-FGA state over time. Capacitance–voltage and photoconductance measurements suggest that the oxides contain a high positive fixed charge—particularly after a 1100 °C N_2 anneal—which aids the passivation of n-type and intrinsic silicon but harms the passivation of low-resistivity p-type silicon.**

Index Terms—**Annealing, passivation, photoconductance, silicon dioxide, surface recombination velocity (SRV).**

I. Introduction

The PASSIVATION attained by a thermal silicon dioxide (SiO_2) layer on silicon (Si) is well known to lead to a low surface recombination velocity (SRV). An SRV of ∼30 cm/s has been attained after a postoxidation anneal in argon and a forming gas [1]; however, as such high temperatures and long oxidation times are required, the process to achieve a low SRV is expensive relative to the cost of modern solar cell processing. Therefore, in recent years, there has been much interest in alternative passivating layers such as hydrogenated amorphous silicon nitride (SiN_x : H) [2], amorphous silicon [3], and aluminum oxide [4].

An inexpensive passivating layer might also be achieved by a chemical oxidation process. In 2003, Kobayashi *et al.* [5] used a concentrated (68 wt%) nitric acid as the oxidizing chemical and demonstrated that very low leakage current measurements, equivalent to that of thermal SiO_2, could be achieved for ultrathin (∼1.5 nm) SiO_2.

In 2005, Imai *et al.* [6] developed a two-step HNO_3 oxidation method, where Si is immersed in a 40-wt% HNO_3 solution at ∼ 110 °C for 10 min followed by immersion in a 68-wt% HNO_3 solution at ∼ 120 °C to form thicker (> 1.5 nm) SiO_2 layers. It was found that the leakage current density was significantly lower than that of the ultrathin 1.5-nm HNO_3 oxide developed by Kobayashi *et al.* Imai *et al.* also showed that a postmetallization anneal in hydrogen at 250 °C further reduced the leakage current due to a reduction in interface states by hydrogen.

Very recently, Mihailetchi *et al.* [7] have passivated boron-doped emitters using an ultrathin oxide grown in HNO_3, which is similar to that developed by Kobayashi *et al.* After adding a SiN_x : H antireflective layer and annealing at high temperature for a short period, emitter saturation current densities J_{oe} as low as 23 fA/cm^2 could be attained. Without the ultrathin oxide layer, J_{oe} could not be measured due to insufficient passivation.

In our survey of the literature, the leakage and J_{oe} of the HNO_3-grown SiO_2 layers have been previously investigated; however, the SRV and the interface trapped charge have yet to be examined, both of which are significant parameters for any surface passivation study. This letter investigates the latter two parameters associated with SiO_2 grown by the two-step process, developed by Imai *et al.*, after the following: 1) no anneal; 2) a nitrogen (N_2) anneal; and 3) a nitrogen anneal followed by a forming gas anneal (FGA). Photoconductance measurements are conducted to determine the SRV of the samples, and capacitance–voltage (C–V) measurements are conducted to assess the oxide thickness, the density of interface states, and the charge density.

II. Sample Fabrication

Nitric oxidation was evaluated on 200-μm-thick 100-mm-diameter single-crystalline (100) oriented FZ 1-$\Omega \cdot$ cm n-type silicon wafers. Prior to oxidation, all wafers received a HF : HNO_3 etch for 3 min to remove saw damage from the surfaces and cleaned by the conventional RCA procedure [8].

The samples that were prepared for photoconductance measurements were immersed in a 40-wt% HNO_3 solution (with a total impurity level of less than 0.0013%) at 108 °C for 10 min followed by a 3-h immersion in a 68-wt% HNO_3 solution at 121 °C, to form $SiO_2/Si/SiO_2$ structures. Some wafers were subsequently annealed in a tube furnace at 800 °C and 1100 °C in N_2 for 30 min with and without subsequent FGA at 400 °C for 30 min.

Samples for C–V measurements were prepared identically, except that following the anneal, the SiO_2 was removed from the rear surface via HF fuming, and 100 nm of aluminum (Al) was evaporated onto the rear to enable ohmic contact with the silicon substrate. Finally, 0.70-mm-diameter contacts were deposited on the front surface to form conventional metal–oxide–semiconductor structures. From the C–V measurements, the oxide thickness (after a high-temperature N_2 anneal) was calculated to be ∼5 nm by the method developed

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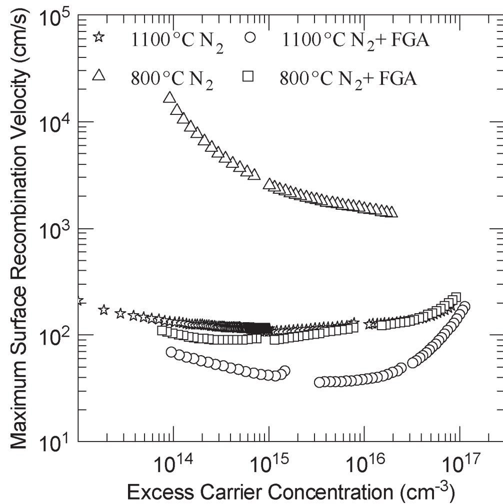

Fig. 1. Maximum SRV directly after the annealing process. For clarity, the figure plots every fifth data point.

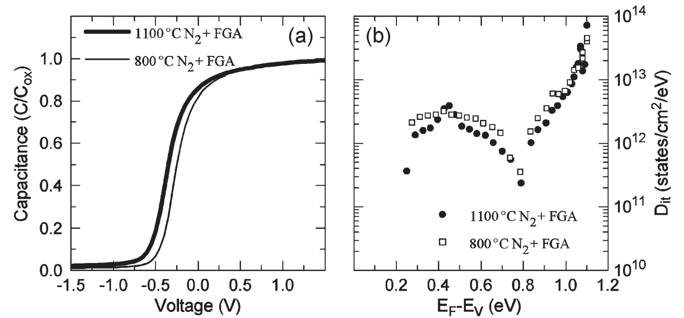

Fig. 2. (a) C–V curves after annealing at 800 °C and 1100 °C in N_2 followed by a 400 °C FGA. (b) Corresponding density of the interfacial defects as determined by Terman analysis.

by Ricco *et al.* [9]. We have assumed the oxide permittivity to be the same as that of a thermal oxide, based on the results obtained by Imai *et al.* [6].

III. Results

A. Photoconductance Measurements

The SRV was determined from the photoconductance measurements using a generalized analysis [10]. Two light sources were employed: a Quantum Qflash X2 lamp used in the WCT-100 instrument [11] and a LED array of wavelength 870 nm. The LED array had several advantages over the Qflash: It operated at one wavelength, simplifying the analysis, the pulse shape was controlled to permit rapid averaging, and a self-consistent technique could be applied to calibrate the light intensity [12], [13]. It could not, however, attain an illumination intensity that is as high as the Qflash. The photogeneration rate from the flash source was corrected to agree with that of the more accurately calibrated LED source.

The SRV plotted in Fig. 1 was calculated from the effective lifetime accounting for the nonuniform carrier concentration in the wafer and assuming an infinite bulk lifetime. The SRV is, therefore, an upper limit to its actual value, but would be overestimated by no more than 18% if the bulk lifetime were 2 ms (a more realistic lifetime of FZ silicon). The figure indicates that, at $\Delta n = 10^{15}$ cm^{-3}, an SRV of less than 42 cm/s was achieved after annealing at 1100 °C in N_2 followed by a 400 °C FGA. This compares to an SRV of ~30 cm/s at the same injection level for a thermal oxide grown at 1050 °C, with a postoxidation anneal in argon for 1 h followed by a 450 °C FGA [1]. Unfortunately, the improvement in surface passivation achieved by the FGA is temporary, presumably due to the instability of the Si–H bond [14], resulting in an increase in the lowest SRV from 42 to 82 cm/s at $\Delta n = 10^{15}$ cm^{-3} one month after the anneal.

B. C–V Measurements

The C–V curves were recorded at 1 MHz using a 4284A precision LCR meter. The measurements were hampered by a significant leakage through the thin oxide, limiting the D_{it} analysis to only those samples that had an anneal in N_2 and a subsequent FGA, indicating that the leakage is dependent on the passivation of interface states, in agreement with the results of Kobayashi *et al.* [5] and Imai *et al.* [6]. The C–V curves presented in Fig. 2(a) are those of the samples annealed at 800 °C and 1100 °C in N_2 followed by a 400 °C FGA. They show two interesting effects: The first is a voltage translation, which relates to a difference in the oxide charge density Q_{ox}, and the second is their similar shape, which indicates a similar density of interface states D_{it}.

The oxide fixed charge is located near the Si/SiO_2 interface and can be either positive or negative; however, for thermal oxides, the positive charge is the more common [15]. If the charge in our samples is located at the interface itself, the shift in flatband voltage equates to Q_{ox} of the 1100 °C sample being 7×10^{11} cm^{-2} $\pm 30\%$ more positive than Q_{ox} of the 800 °C sample.

While there is a clear difference in Q_{ox} between the C–V curves, their shape is very similar, implying that their D_{it} is also similar. Fig. 2(b) plots D_{it} as a function of energy above the valence band, as calculated by Terman's analysis [16], indicating that the 1100 °C sample has only slightly fewer interface states than the 800 °C sample.

We conclude from the C–V measurements that the lower SRV attained at higher temperatures relates mostly to more positive fixed charge rather than lower D_{it}.

C. Surface Passivation versus Immersion Time in the 68-wt% HNO_3 Solution

In a previous work on thin SiO_2 layers grown in nitric acid, the growth rate depended linearly on the immersion time in the 68-wt% HNO_3 solution [17]. Here, we investigate how SRV depends on immersion time. Fig. 3 plots the results for both n- and p-type silicon of low and high resistivity after a 1100 °C N_2 anneal. It shows that the SRV decreases rapidly for short immersion times and saturates after 3–4 h. The figure also shows that SRV depends on substrate doping, most likely due to the positive Q_{ox} at the interface as now explained. On low-resistivity p-type silicon, the positive charge attracts the minority carriers (electrons) and repels the majority carriers (holes), increasing the recombination rate and, therefore, the SRV, due to insufficient inversion at the interface [15]. On

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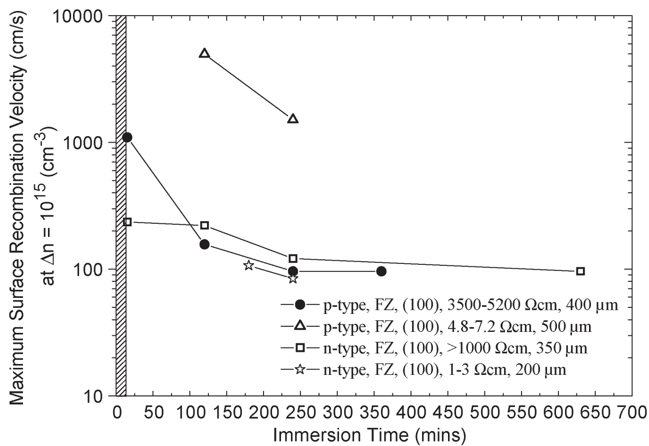

Fig. 3. SRV as a function of immersion time. The shaded area corresponds to the time spent in the 40-wt% nitric acid solution. The unshaded area corresponds to the immersion time in the 68-wt% nitric acid solution after being immersed in the 40-wt% solution. All samples received a 1100 °C N_2 anneal for 30 min but not an FGA.

high-resistivity (near intrinsic) p-type silicon, the positive charge is sufficient to cause substantial inversion, and the samples behave similarly to those of high-resistivity n-type silicon, i.e., the dopant concentration in these samples is too low to affect the measurements. On low-resistivity n-type silicon, the positive charge repels the minority carriers (which were already low to begin with), making the recombination rate still lower. This dependence of the SRV on the substrate doping would be exacerbated by the asymmetric capture cross sections frequently observed at SiO_2-Si interfaces, whereby the electrons are more readily captured than the holes [18].

IV. Conclusion

This letter has presented the first study of the SRV attained by nitric acid oxides. Without an anneal, the two-step nitric oxide of Imai *et al.* offered poor passivation, but, after a high-temperature anneal in N_2 and an FGA, an SRV of 42 cm/s (at $\Delta n = 10^{15}$ cm^{-3}) was attained, which is similar to that of a thermal oxide. C–V and photoconductance measurements suggest that the oxides contain a high positive fixed charge—particularly after a 1100 °C N_2 anneal—which aids the passivation of n-type and intrinsic silicon but harms the passivation of low-resistivity p-type silicon. It has been also shown that the SRV saturates after 3–4 h of immersion in the 68-wt% nitric acid solution and that the benefit of the FGA is mitigated over time.

In this letter, the high-temperature anneal has been performed in a tube furnace, making the procedure no less expensive than the conventional tube oxidation. Having demonstrated the potential of nitric oxidation, attention can now be paid to replacing the tube anneal with a rapid thermal anneal. If successful, nitric oxidation could provide an inexpensive means to attain good passivation for solar cells or lifetime test structures.

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