

TOWARDS A SIMPLIFIED 20% EFFICIENT SLIVER CELL

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ABSTRACT

Sliver technology, first developed at the ANU, offers large reductions in silicon consumption and wafer throughput per MW. However, sliver technology requires more processing steps than conventional silicon solar cell fabrication, and thus fabrication represents a larger cost per wafer. This additional cost is easily justified because sliver cells are highly efficient and also the module area producible per wafer is far greater than for conventional technologies. Current research at the ANU is aimed at delivering a simplified processing sequence capable of producing sliver cells with a reduced manufacturing cost and with better performance than the originally developed fabrication process. With the simplified process it should be possible to reliably manufacture > 20% efficient cells with a high yield.

SLIVER SOLAR CELLS

The sliver cell and the sliver technology were invented [1] and developed [2-5] at the Australian National University with support from Origin Energy. A sliver cell is a very thin, monocrystalline silicon solar cell. The technology allows for large decreases in silicon usage, by a factor of 10-20, and a large reduction in the numbers of wafers processed per module, by a factor of 20-50, compared with standard silicon technology.

The essential step in forming slivers is the micromachining of deep, narrow grooves all the way through thick silicon wafers. The wafer is then processed using standard techniques to turn each of the slivers into a solar cell. Completed cells are removed from the wafer and rotated through 90 degrees to give a large area multiplication. The large face of the sliver cell, the sidewall formed by grooving, becomes the sun-facing surface of the cell, whilst the metallised contacts run along either edge. The processing treatment of both sidewalls of a sliver is identical and so the cell is perfectly bifacial. Figure 1 represents a wafer in which sliver cells have been processed. Typical sliver dimensions are 50-100mm long, 0.5-2mm wide and 40-60µm thick.

There is virtually no shading due to metallisation since the metal contacts are on the side of the sliver. The metal contacts occupy only a small fraction of the total surface of the cells, and doping below the contacts can be made quite heavy. Excellent, low resistivity contacts and minimal recombination are thus achieved. Good short-circuit currents, open-circuit voltages and efficiencies are observed as a result. Efficiencies above 19% were already

achieved using the original sliver cell processing sequence developed in 2002-3.

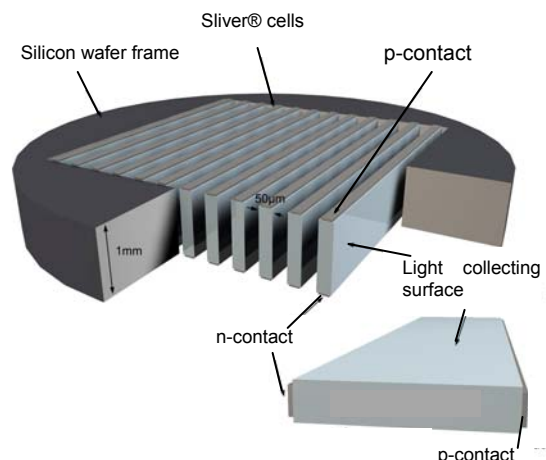


Fig. 1. Each wafer can contain several thousand slivers with an effective combined surface area of 20-50 times the wafer surface area.

The long and narrow shape of sliver cells confers unusual possibilities for module designs. One such design, utilises a very simple lambertian reflector, and has cells occupying only a fraction (typically half) of the module surface area [6]. This allows for a further reduction in silicon usage.

SIMPLIFIED SLIVER PROCESSING

Complex wafer processing is more expensive because it entails a larger fabrication facility, more processing equipment, higher maintenance costs and larger consumables and waste disposal costs. Also, the longer the processing sequence the lower the yield will be for a similar but shorter sequence. A further disadvantage of a long process compared with a short process is that development and refinement of the process is more difficult: feedback takes longer, and the problem of lower yields commonly encountered in R&D is exacerbated.

The original sliver cell processing sequence consists of 59 separate processing steps [7], where a single processing step is defined as a set of operations that take place with the assistance of a particular piece of process equipment (such as a phosphorus diffusion) or which are similar and occur sequentially (such as a wafer-washing step). Recent research at ANU has focused on arriving at a simplified processing sequence capable of delivering higher efficiency cells and a higher yield. The simplified processing sequence contains far fewer processing steps,

around 32 of the same type of steps, and utilises fewer pieces of equipment.

Texturing is quite easily added to the process, though standard texturing techniques can not be applied to anisotropically etched sliver cell's <111> sidewalls. Excellent texturing and light-trapping is instead achieved via an acid etch technique through a very thin LPCVD deposited silicon nitride layer. Incorporation of texturing and an optimal ARC will result in sliver cells capable of delivering efficiencies greater than 20% at one sun.

SLIVER CELL DESIGN REQUIREMENTS

Sliver cells have several specialised design features and requirements. Since the cells are very thin (around 50 μm) with emitter diffusions on both the front and rear surfaces, very high internal quantum efficiencies and also high open-circuit voltages are possible with only relatively small minority carrier diffusion lengths in the bulk. This is most fortuitous since the distance between sliver cell terminals is large enough (in the order of 1000 μm) for majority carrier drift in the bulk region to contribute significantly to series resistance losses unless low resistivity substrates (which have reduced diffusion length) are used. Modelling has been used to demonstrate that 0.1 $\Omega\cdot\text{cm}$ boron doped FZ wafers give good results in respect of minimising both bulk series resistance and bulk recombination [8].

A major loss mechanism for sliver cells is related to the resistance of the emitter region. This manifests itself as a distributed series resistance and generally has the largest impact upon performance for an otherwise well made cell. Modelling has previously been used to show that this is the case [8], and that it is particularly prevalent for either wide sliver cells or for sliver cells operating under concentrated illumination. Even at an illumination intensity of one sun for 1mm wide cells, the series resistance of the emitter regions alone can account for some 3 or 4 fill-factor points

A closely related loss mechanism which has been observed in sliver cells fabricated with the simplified process is attributable to a region of heavily compensated silicon which arises due to the overlap of the phosphorus sidewall emitter diffusion with the sliver cell edge boron diffusion. The consequence is a reduced fill-factor and open-circuit voltage, corresponding to a distinct non-ideal recombination component. This is readily observed on a measured $J_{\text{SC}}-V_{\text{OC}}$ curve. On the other hand, the close proximity of the two diffusions provides a low reverse breakdown voltage owing to tunnelling, which confers robust tolerance of partial shading of a module, without the need for bypass diodes.

MONITORING SIDEWALL EMITTER DIFFUSIONS

Effective monitoring and tight control over the sidewall emitter diffusion is crucial in achieving optimal sliver cells. Diffusion doping is traditionally measured by including one or more lightly doped, undiffused monitor wafers in each diffusion. The sheet resistance is then simply measured using the four point probe method. If the diffusion process is not limited by the arrival of diffusion reactant gases then it can be reasonably assumed that every surface receives

the same dose as the monitor wafers. However, this proves not to be the case for the doping of sliver cell sidewalls. In this case, the arrival of reactant gases during the deposition stage of the diffusion somewhat limits the available supply of dopant atoms at the silicon surface and results in lighter diffusions. The sidewall emitter diffusion therefore requires separate monitoring. We include a specially fabricated sidewall monitor wafer with the phosphorus emitter diffusion. This undiffused p-type wafer has etched grooves the same as those wafers containing sliver cells. The individual strips of silicon are, at the end of the diffusion and drive-in, removed and the sheet resistance measured using a four-point probe as shown in figure 2.

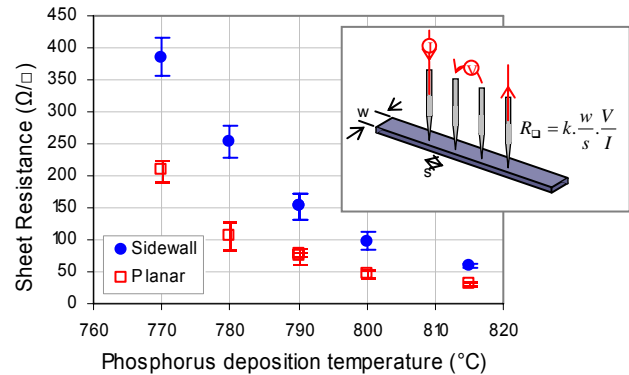


Fig. 2. Sidewall and planar diffusion sheet resistances, and sidewall measurement technique (inset).

Also plotted in figure 2 are sidewall sheet resistance measurements for experimental 1mm thick wafers with approximately 80 μm wide grooves, along with the accompanying measurements for planar wafers. The wafers are from six separate diffusions, conducted at varying deposition temperatures (two were done at 790°C). These, and other measurements, indicate an approximate two-fold increase in emitter sheet resistance on sliver sidewalls compared to planar wafers. The additional sheet resistance increases for thicker wafers and for narrower grooves.

To complete the picture it is necessary to measure how the doping, or sheet resistance, varies across the 1mm width of the diffused sidewall. A lengthy process, involving the creation of a number of very small channels at various positions on the sidewall of the monitor strips, is used to isolate parts of the sidewall surface. The sheet resistance is thereby measured at specific locations. Observed sheet resistance profiles for four different diffusions are plotted in figure 3. The dashed line accompanying each set of measurement points corresponds to the sheet resistance measured for the complete sidewall surface. Doping at the middle is marginally lighter than at the edges, but generally the dose is quite uniform across the sliver cell sidewall for the particular diffusion conditions that we use.

Accurate monitoring and control of the emitter diffusion is especially important for wider cells (1.5mm or 2mm wide for example) and for sliver cells that are designed for operation at low to medium concentration ratios [8].

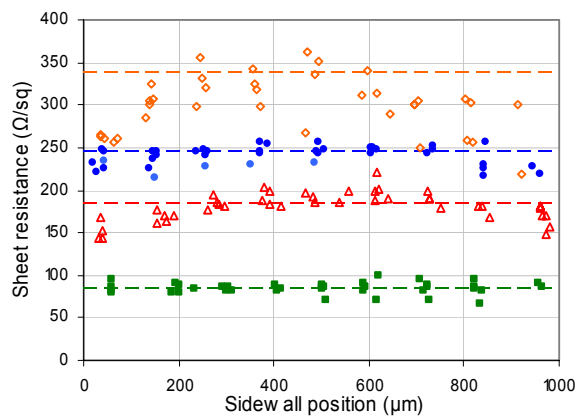


Fig. 3. Measured emitter doping profile across sliver sidewalls.

CELL PERFORMANCE FROM SIMPLIFIED PROCESS

During the development of the simplified processing sequence, cells produced were all un-textured and most had a silicon dioxide AR coating. This was partly for ease of processing and then later was done out of necessity whilst the laboratory's LPCVD furnace was completely rebuilt. A history of the development of the sequence is presented in figure 4. This plots the achieved efficiency, for each completed batch, on a time scale spanning the development of the simplified processing sequence.

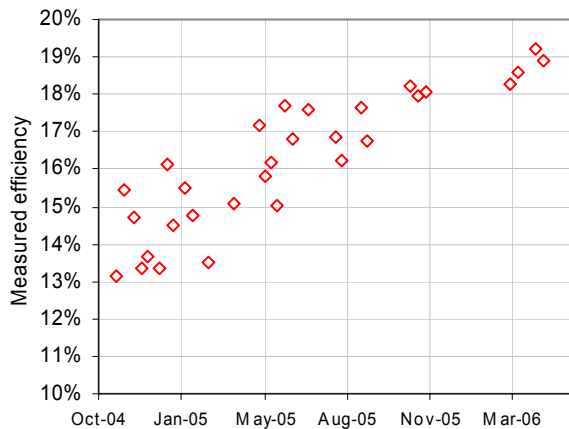


Fig. 4. Achieved efficiencies, without texturing, over the course of streamlined fabrication process development.

Much of the development of the sequence involved dealing with parasitic series and shunt resistance, altering diffusion recipes, devising an improved metallisation scheme and changing around the order of process steps in order to maximise yield. The gains in efficiency are made via incremental improvements in open-circuit voltage (now 660mV – 670mV at one sun) and significant improvements in fill-factor (now at 0.81 or above). What the plot does not show is that, on top of the gradual improvement in efficiency, there is also a large improvement in reliability and consistency of results both within and between batches. Batches now have very high yield, with performance of all cells matching very closely. This accomplishment within an R&D setting bodes well for the robustness of the process sequence in a manufacturing environment.

The best untextured 1mm wide one-sun cells produced with the simplified processing sequence have efficiencies of up to 19.3% (calibrated in-house measurement). A short-circuit current density greater than 36.5mA/cm² would be required to satisfy the 20%+ efficiency mark. Such a current density is believed to be easily achievable in the near term with good acid-etch texturing. The best cell efficiencies at high illumination intensities are found for narrow cells with heavy emitter doping. Cells with efficiencies above 18.6% over an intensity range of 5 – 15 suns and cell with efficiencies above 18.3% between 30 and 50 suns have been produced. These should also translate to >20% efficiency with the addition of texturing.

Some insight into the influences on cell behaviour can be gained by examining a contour plot of measured efficiency against sliver cell width and illumination intensity (figure 5). This plot was constructed from measurements of cells that were fabricated as a single batch using five wafers of differing thicknesses. The batch produced good cells, although the short-circuit current was a little low for the cells of width around 700μm. The upper right-hand corner of the plot is a region dominated by series resistance related to the emitter diffusion. For wide cells this region clearly commences at only a few suns. Lighter emitter diffusions would see the influence even more apparent at one-sun. Efficiency drops away at low illumination intensities due to a combination of lower open-circuit voltage and also reduced fill-factor owing to non-ideal recombination. This is particularly apparent for narrow cells where the emitter diffusion is heavier in the vicinity of the adjacent p-contact edge boron diffusion. The ridge of high efficiencies essentially corresponds to a high fill-factor where non-idealities and series resistance both have minimal influence. The location of this ridge is to a fair degree controlled by the emitter diffusion.

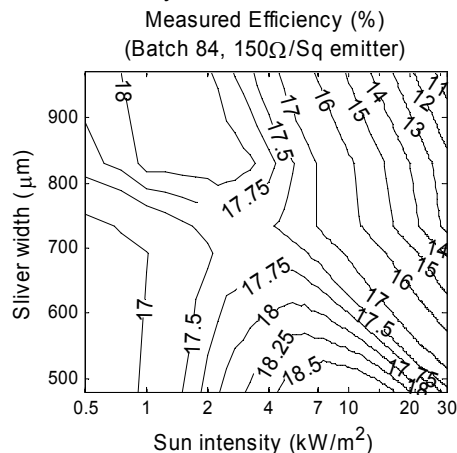


Fig. 5. Measured efficiencies of cells (SiO₂ ARC, no texturing) fabricated with various widths and tested across a range of illumination intensities.

In a similar manner, a batch has been produced using 1mm thick wafers but with a range of different emitter diffusions. The phosphorus deposition temperature is varied in each case. This batch was not as good as the best ones produced and the short-circuit current density for cells with heavy diffusions was lower than measured in other cases. Nonetheless, the contour plot of figure 6

highlights how sensitive cell performance can be to emitter doping. Fill-factor quite rapidly drops away with increasing sheet resistance. On the other hand, non-ideal recombination limits fill-factor if diffusions are too heavy.

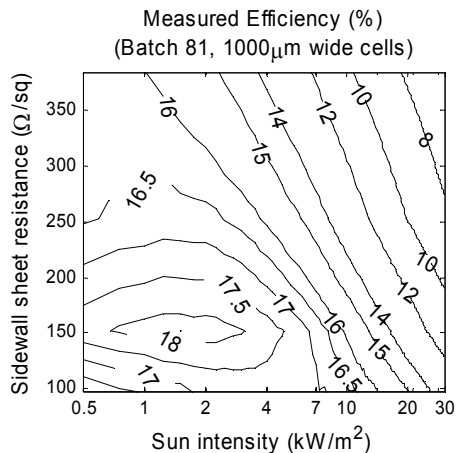


Fig. 6. Measured efficiencies of 1mm wide cells (SiO_2 ARC, no texturing) fabricated with various emitter diffusions and tested across a range of illumination intensities.

SLIVER WAFERS TO SOLAR MODULES

Near the end of wafer processing, each 15cm wafer contains up to several thousand slivers, enough to cover up to 1m^2 of module area. The small size of each sliver necessitates a novel module construction method.

A method of packaging Sliver solar cells has been devised that appears to have considerable advantages over previous techniques. As far as possible the method takes advantage of standard PV modularisation technology. The only materials used in the module are those found in the great majority of conventional PV modules. The module design is sufficiently close to conventional module designs that we have confidence that it will have similar reliability to conventional modules.

THE COST OF ENERGY FROM SLIVER CELLS

We have modelled the expected cost of sliver modules for a mature streamlined sliver cell and module fabrication process [9]. The model compares current conventional PV technology with mature sliver technology expected to be available within a few years following thorough process engineering by an experienced company. Reasonable projections from known technology are assumed. No further breakthroughs are assumed. It appears that a reduction in module cost of up to three quarters is possible, arising from a 10-20 fold reduction in silicon consumption and a 20-50 fold reduction in wafer starts per MW.

ACKNOWLEDGEMENTS

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