SILICON LIQUID PHASE EPITAXY FOR EPILIFT SOLAR CELLS

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ABSTRACT

Silicon liquid phase epitaxy (LPE) is a suitable silicon deposition process for the fabrication of thin film silicon solar cells. In this paper we discuss the design and operation of a batch LPE system which is a first step towards mass production. The issue of melt cost can be addressed by efficient recovery of the melt and by switching to more widely available metals, such as tin. Layers grown by the epilift technique using a tin melt have displayed excellent coverage and morphology. Epitaxial layers can be detached by both chemical and mechanical means, with only minimal consumption of the substrate material.

1. INTRODUCTION

Silicon liquid phase epitaxy (LPE) is a suitable silicon deposition process for the fabrication of thin film silicon solar cells. It has several features which make it attractive for silicon photovoltaics:

- It allows the production of material of excellent quality. Minority carrier lifetimes in excess of 50us can be realised.
- Utilisation of silicon is excellent, with virtually all of the silicon that is used ending up in the epitaxial layer.
- Consumption of process gases (nitrogen and hydrogen) is minimal, and the process gases are relatively benign.

In combination with recently developed lift-off techniques such as the epilift technique [1] which allow high quality, single crystal silicon layers to be grown, cost effective, high efficiency cells can be realised. However, the challenges of high volume deposition and the high cost of the melt still need to be addressed. For the epilift technique, the detachment of the epilayer from the substrate is also a key consideration. These issues are discussed in this paper.

2. EPITAXIAL REACTOR DESIGN

For LPE to become a suitable technique for high volume production of solar cells, significant changes from laboratory-scale LPE systems are required. Batch mode systems appear to offer the best possibility. We have designed and built a vertical batch LPE system, capable of processing up to 10 100mm diameter wafers at a time. A schematic of the system is shown in fig.1. The system features a 5 zone furnace to allow good temperature uniformity to be realised in the melt. Wafers are stacked vertically with a typical spacing of 5mm. This arrangement results in good layer uniformity, maximizes the number or wafers that can be processed in a given volume of melt and allows rotation of the wafers during growth to further improve uniformity and growth speed.

Epitaxial growth is a two step process, involving first the saturation of the melt with silicon, followed by epitaxial growth. This usually means that silicon source wafers are first loaded and used to saturate the melt at the growth temperature. Following saturation, the source wafers have to be unloaded and the substrate wafers are placed in the cassette for growth. We have investigated a modified growth sequence in which the source wafer is placed in the bottom two slots of the cassette and the substrate wafers are placed in the upper slots.

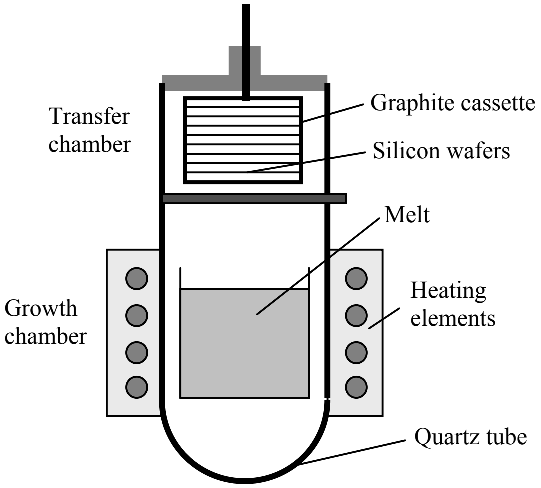

Figure 1: Schematic of the batch LPE system

The growth sequence is as follows:

1) The source and substrate wafers are loaded into the graphite cassette. To ensure that no gas bubbles remain in the gaps between wafers, the wafers are

loaded in at a slight angle of approximately 3°. During loading and unloading, the transfer valve is closed and the growth chamber remains under ultrapure hydrogen atmosphere, at a temperature of 500°C. The hydrogen is purified at point of use with a palladium diffusion cell.

2) The transfer chamber is closed, evacuated to $5x10^{-5}$ torr, and backfilled with hydrogen twice.
3) The transfer valve is opened and the wafers are lowered into a position just above the melt. A quartz baffle positioned above the graphite cassette seals the crucible. The quartz baffle reduces heat loss to from the crucible, improves temperature uniformity within it, and it reduces In evaporation.
4) The temperature is increased to 980°C and allowed to stabilize.
5) The cassette is gradually lowered into the melt. Since the source wafers are positioned at the bottom, they contact the melt first and saturate the melt before the substrate wafers are immersed.
6) Once all the wafers are immersed, growth is commenced by reducing the temperature to 750-800°C, with typical cooling rates in the range 0.5-1.5°C.
7) The cassette is raised just above the melt and rotated rapidly (100rpm) to remove the melt.
8) The furnace is cooled to 500°C. The cassette is raised into the transfer chamber and the transfer valve is closed. Following evacuation and backfill with nitrogen, the transfer chamber can be opened.

The above sequence was found to result in epitaxial layers of reliably good quality and uniformity. The rapid cassette rotation at the end of the growth was found to remove the majority of the melt. However, for complete melt removal, faster rotation will be needed.

The effect of cooling rate and rotation speed during growth have been studied. Best results were obtained with cooling rates around 0.5°C/min and very slow rotation, of the order of 1rpm. Fast rotation leads to turbulence in the melt which generally results in poorer thickness uniformity across the wafer.

3. EPITAXIAL LAYER GROWTH

To date, 'Epilift' epitaxial layers have been grown chiefly from indium. These layers have shown minority carrier lifetimes in excess of 30µs and have been used for the fabrication of efficient Epilift cells [2]. The disadvantage of indium is its limited availability, which could become a significant issue in large volume production. For this reason we have studied epitaxial growth from tin. Cz wafers, oriented 2.5-4° off the (111) plane, were oxidised and various line seed patterns were opened in the oxide to study the morphology of the resulting epilayers. Fig. 2 shows epilayers grown from Sn with line spacings of 400µm and 800µm, respectively. It can be seen that exceptionally smooth epilayers were obtained. Further, it was found that the amount of lateral overgrowth of the epilayer over the oxide was significantly higher for layers grown from tin than from indium. With an effective rear reflector, line spacings up to 800µm appear feasible for epilift cells grown from a tin melt.

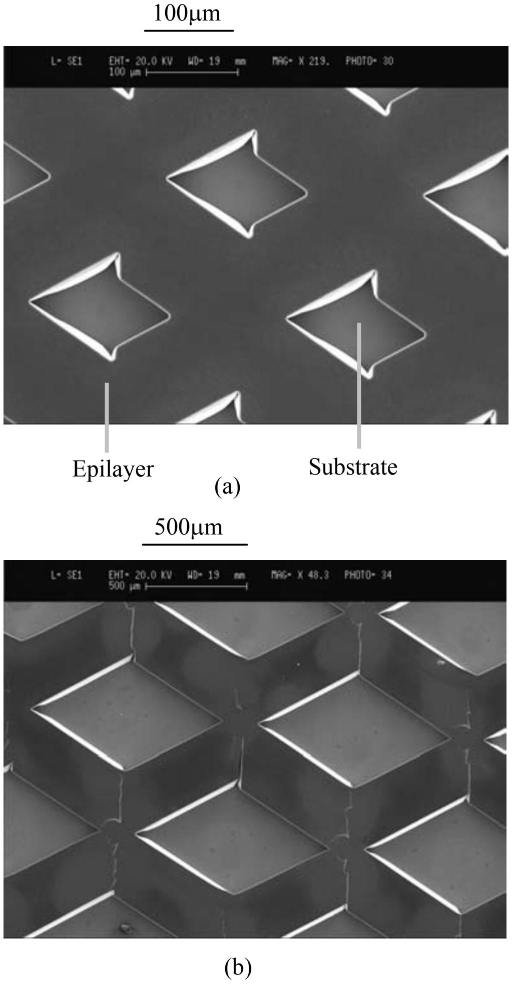

Figure 2: Epilayers grown from a Sn melt using (a) 400µm and (b) 800µm seed line spacing

Occasionally, large line spacings are observed to lead to metallic inclusions in the epilayer, which will be detrimental to cell performance. Inclusions can be avoided by careful choice of the cooling rate. A major disadvantage of the use of Sn is that the minority carrier lifetimes measured on Sn layers to date have been significantly lower than those for In grown layers, with lifetimes usually being 1µs or less. The reason for the low lifetimes is being investigated.

4. DETACHMENT OF EPITAXIAL LAYERS

4.1 Chemical detachment

In order to minimise etching of the epilayer, it is desirable to use a selective etching method. Electrochemical techniques based on the selective etching of p type over n type silicon [3] have been used successfully [1] but are more complex since they require electrical contact to be made to each wafer. An alternative is to use simple selective chemical etch techniques. It is well known, for example, that a solution of 1:3:8 parts of hydrofluoric, nitric and acetic acid etches heavily doped p type silicon much more quickly than lightly doped silicon.

We have systematically investigated solutions consisting of hydrofluoric, nitric and acetic acids and water. WE have found that a solution of 1:1:4 parts of hydrofluoric acid : nitric acid : water displays a substantically better selectivity than the 1:3:8 etch and is suitable for the detachment of epilayers. In order to minimise the etching of the substrate, a lightly doped, n type substrate is used and the top surface is diffused with boron prior to masking and patterning. During detachment, only the heavily boron doped surface layer is etched away, leaving the epilayer and the rest of the substrate virtually unetched.This approach also minimises the creation of nitric oxide in the solution. Nitric oxide is a strong oxidizing agent and leads to a reduction in the etch selectivity.

Another approach is to grow a p^+/p epitaxial structure. Using boron as a dopant during LPE growth, such a structure can be fabricated in a single growth step [4]. The above approaches are illustrated in fig. 3.

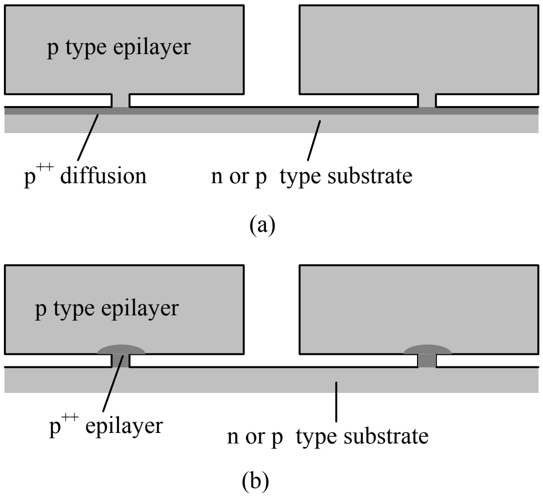

Figure 3: Approaches to the chemical detachment of epilayers which minimise etching of epilayer and substrate. (a) epilayer grown on a p^{++} diffused, lightly doped substrate, (b) p^+/p epi structure on a lightly doped substrate.

4.2 Mechanical detachment

Mechanical detachment is an attractive alternative to the current detachment method based on chemical etching. A major challenge for mechanical detachment is the need to make strongly bond the epilayer to a suitable superstrate without also bonding the substrate, since any adhesive which flows through the holes and contacts the substrate will bond equally well to it as to the epilayer. In several experiments, photoresist was used instead of SiO_2 as the masking material for epitaxial growth. High temperature treatment 'carbonises' the resist [5]. The resulting carbonized resist layer has weak adhesion to the silicon substrate. During detachment, the adhesive can bond to both the epilayer and carbonized resist, leading to their detachment from the substrate. To date small area epilayers of several cm^2 have been detached with this technique. The technique appears to be easily extendable to larger areas. Fig. 4 shows an epilayer grown on carbonized resist.

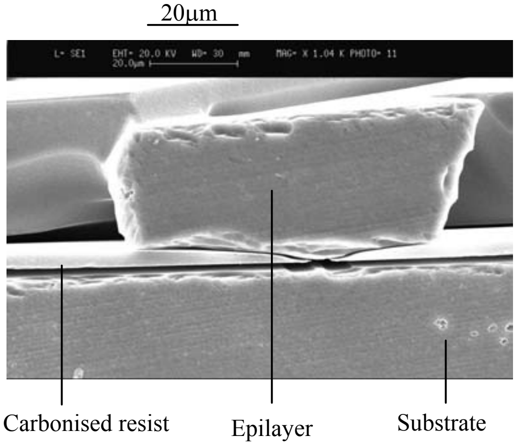

Figure 4: Cross section SEM micrograph of an epitaxial layer grown on a carbonized resist masking layer

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